Pulsonix FPGA Interface

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Pulsonix includes as standard, additional features to aid the use of Field Programmable Gate Arrays (FPGA) and the increasing large pin counts associated with this type of device. The FPGA interface is supplied as a standard interface free of charge within the Pulsonix environment. Most of the major FPGA manufacturers provide their own tools for designing the logic and performing the pin assignments necessary with an FPGA. Interface features are provided that allow the integration of these tools and the data they generate directly in to the Pulsonix system.

Pulsonix will directly support formats for Altera's Quartus II development system and the Xilinx ISE development system (other system interfaces are scheduled for developed). Please contact our technical support desk or your local distributor if you would like to register your system. Pulsonix also writes and reads Part Pin CSV format files, this generic format can also be used in the FPGA environment by some systems.

The Process Flow

FPGA pin assignment data generated by manufacturers' tools can be imported into a part in the Pulsonix library. From there, it can be included with the part into the schematic and propagated forwards to the PCB layout. You can also start from within the Pulsonix Part editor and export the Part pin data to a CSV format file for use with the FPGA tool.

In parallel, you can develop your FPGA internal functionality using the Altera and Xilinx development tools. Once completed, or even part completed, write out an ASCII file. Changes to the FPGA pin out can be quickly reloaded into Pulsonix reducing the need for error prone manual editing.

Reports about pin swaps performed in the Pulsonix PCB will include additional FPGA information to assist with the process of updating the corresponding pin assignments in the FPGA design system.

Multiple FPGA implementations may be retained as separate Parts in the Pulsonix library. The Pulsonix Part used in the design is then replaced using the new pin mappings to complete the process. This can be an iterative process and run multiple times to completion of the finished FPGA device.

Importing FPGA Pin Data

FPGA pin information can be read into a Pulsonix Part to construct the FPGA pin data using the Import Pin Data option or using Copy/Paste from a spreadsheet. Additional checks for the Part to gate pin mappings are available by using the Check Pin Mappings option.

Altera PIN file format

The Altera Quartus II software will automatically generate a .pin ASCII format file as Part of the FPGA design process. This file contains pin assignments and other pin information for an FPGA design.

Importing a Altera PIN file will assign the Pin Name/Usage values from the file to the Logic Name fields of the Pulsonix Part pins by mapping the Location values from the file to the Pulsonix Part pins' Pin Name fields.

Xilinx PAD file format

A .pad ASCII format file can be generated by the Xilinx ISE software as part of the FPGA design process. This contains the I/O pad assignments and other properties.

CSV file format

Pulsonix FPGA also supports import and export of Part pin data in standard .csv format. When the CSV file includes the Logic Name field the Part will be set as a FPGA.

Back Annotation Report

During PCB layout some pin swaps may occur. The Pulsonix Back Annotation report shows what pin swaps have been made. For an FPGA part, this will additionally show the pin Logic Name representing the FPGA pin name as a guide to making the equivalent change in the FPGA design system.

Feature Summary:

- Supplied free-of-charge as part of Pulsonix
- Integrated within the Pulsonix design environment
- Supports Industry Standard FPGA design tools
- Supported in Pulsonix Schematic and PCB design editors
- Can be used as parallel design process with FPGA tool
- Top-down or bottom-up design process possible
- Start within FPGA design tool
- Start by using Pulsonix Parts
- Easy bi-directional transfer of FPGA data
- Parts used in design marked as 'FPGA' type
- Back annotation data of pin swaps reported
- Supports Altera Quartus II design tool
- Supports Xilinx ISE design tool
- Supports 'generic' CSV format files

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