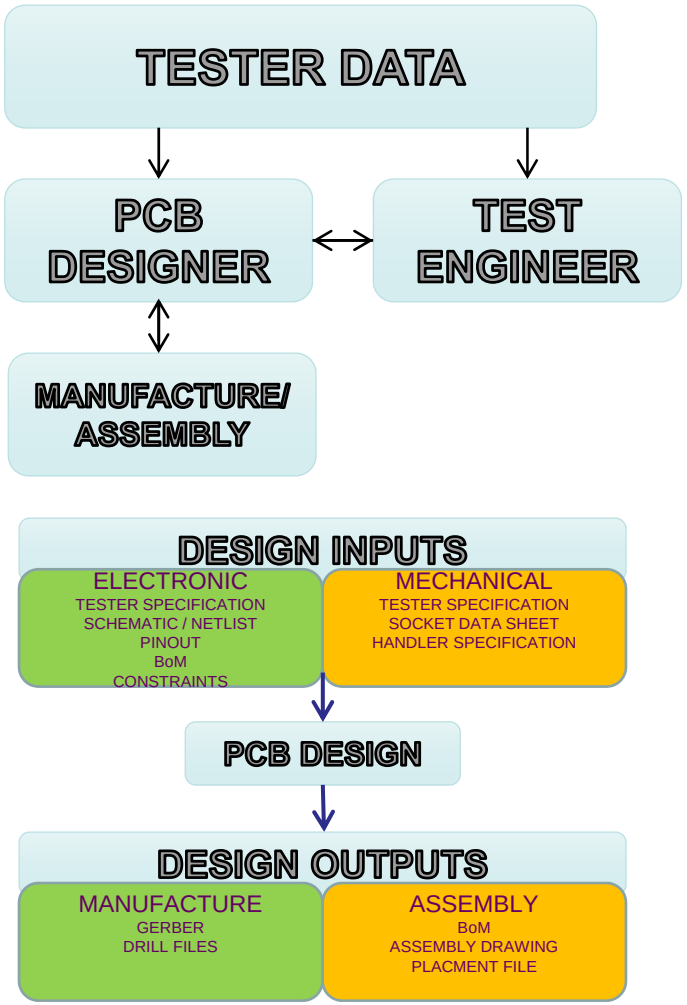
Design Engineering, Layout & Simulation

Date: 18/09/12

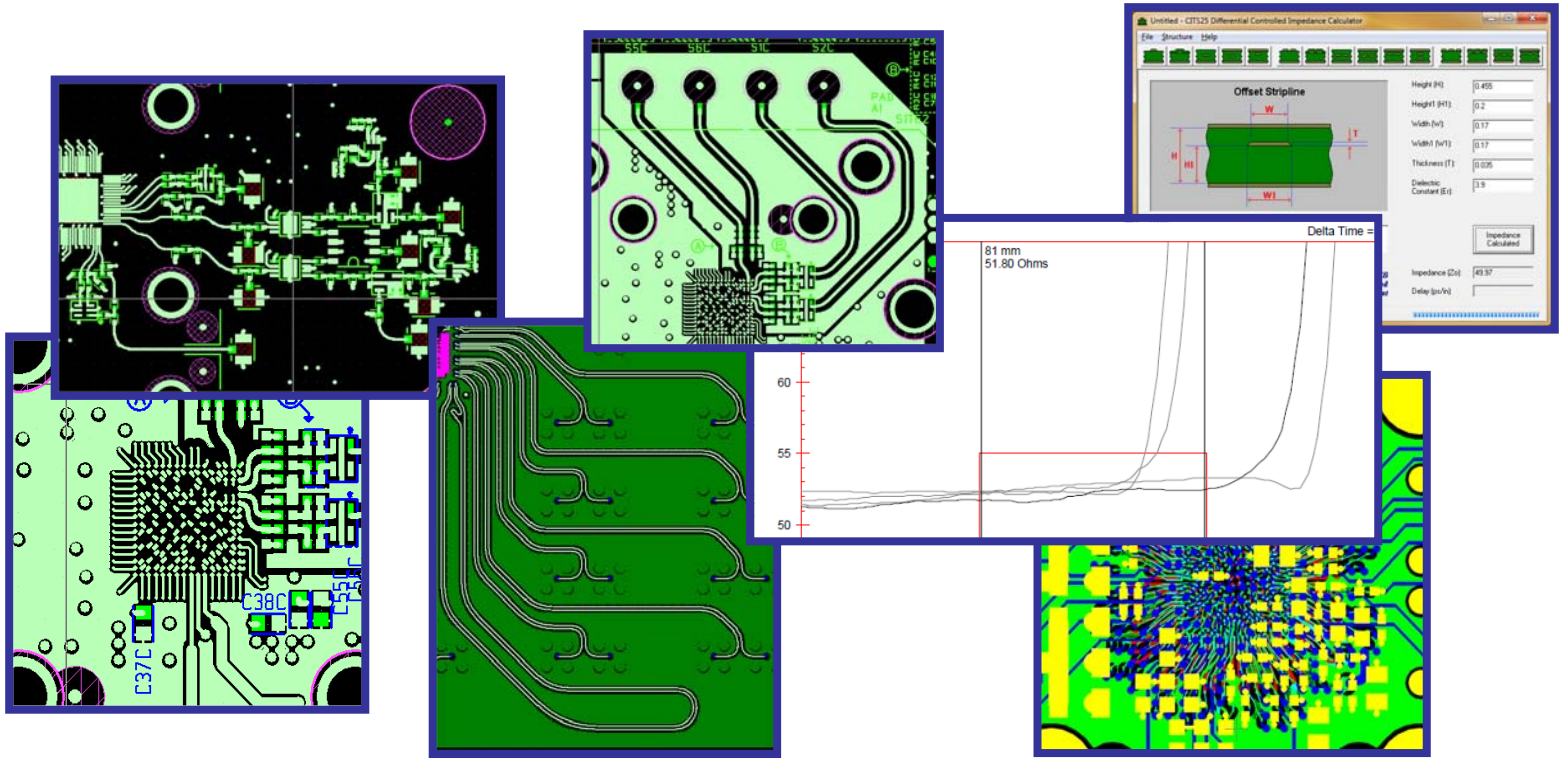
Design Engineering Overview

- PCB Design is an important part of the project as it is the link between the electronic and physical parts.
- This puts the PCB designer in a position where they are having to find the best solution which meets all the requirements of the Test Platform, Test Engineers, Manufacturers and Assemblers.
- With increasing complexity in the projects comes a greater chance of conflict between these requirements.
- Our understanding of the complete PCB design process and PCB manufacturing process will help eliminate any possible conflicts, reducing design time and maximising the manufacturability and ruggedness of the PCB.
- Our experience of RF, High Speed Digital and Analog design supported by Simulation enable us to deliver the required electrical performance of the PCB.

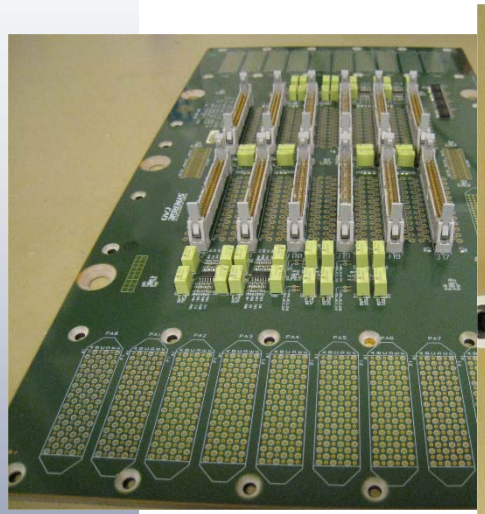


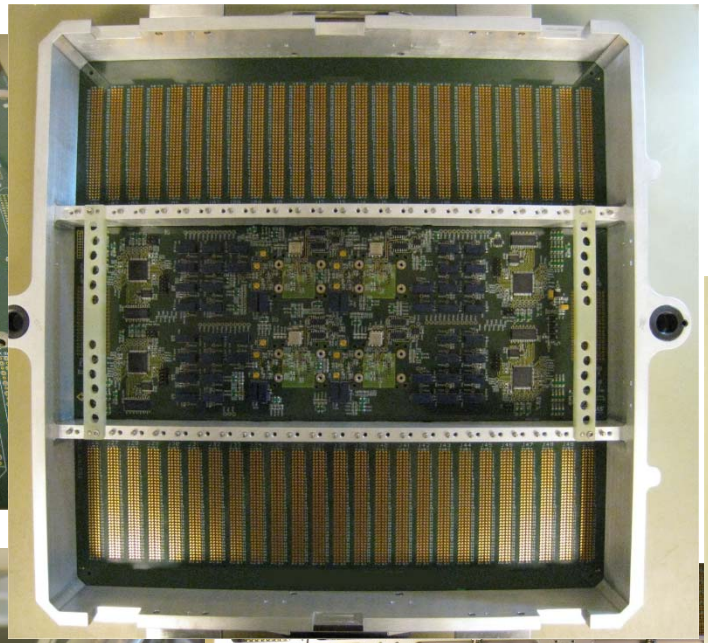
Design Engineering
Schematic Capture and Layout Experience

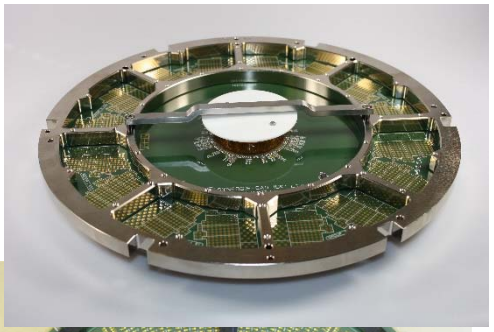
- Combined our design engineers have a broad background and experience in RF Microwave, Electronics, Chemistry, Mechanical engineering and PCB Layout.
- As a brief summary of our design experience includes:
  - uBGA, RF, High Speed Digital, Analog, Mixed Signal designs.
  - Complex board builds, blind, buried, micro vias, multiple laminations and combined materials.
  - Impedance controlled: Differential, Single ended, Stripline and Surface Microstrip, Embedded Microstrip,.
  - Mechanical: Sockets, Shielding, Systems, Custom Stiffeners, Cables.

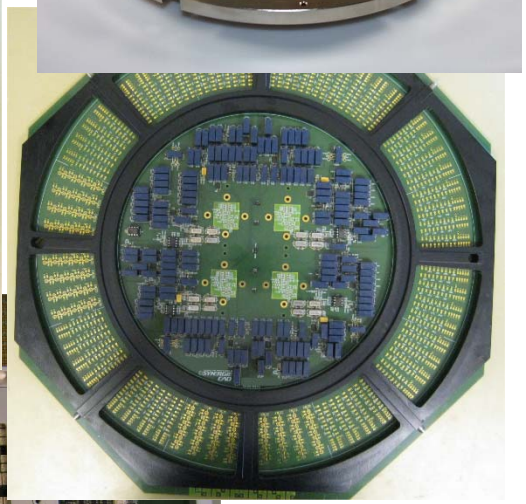


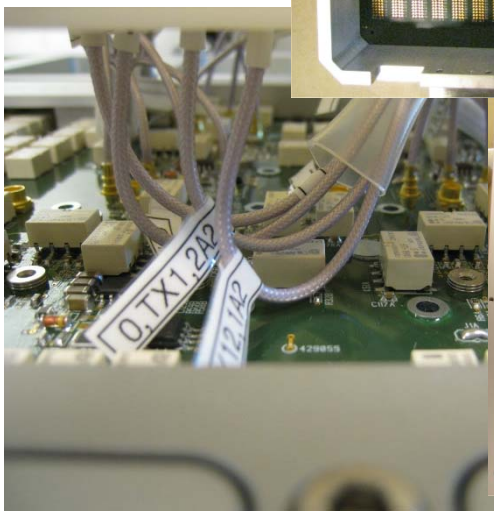
Examples - Design Engineering - Test Interface Boards
Design, Manufacture, Assembly and Test

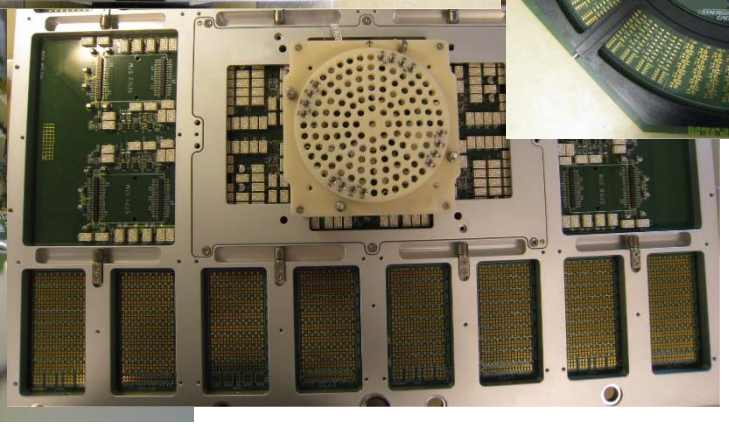












Only a very small sample of boards Designed and Manufactured.

Design Engineering
Simulation Overview - Tool Set

- ANSYS HFSS software is the industry-standard simulation tool for 3-D full-wave electromagnetic field simulation and is essential for the design of high-frequency and high-speed circuit design.
  - Provides accuracy for the design of high-speed circuits, test sockets, PCB interconnects, high-frequency components and RF/microwave components.
  - Evaluate signal quality, including transmission path losses, reflection losses due to impedance mismatches, parasitic coupling and radiation.
  - Visualize 3-D electromagnetic fields.

- ANSYS SIWave to analyse complete designs (includes multiple, arbitrarily shaped power/ground layers, vias, signal traces and circuit elements).
  - Perform complete signal-integrity and power-integrity analysis from DC to beyond 10 GHz.

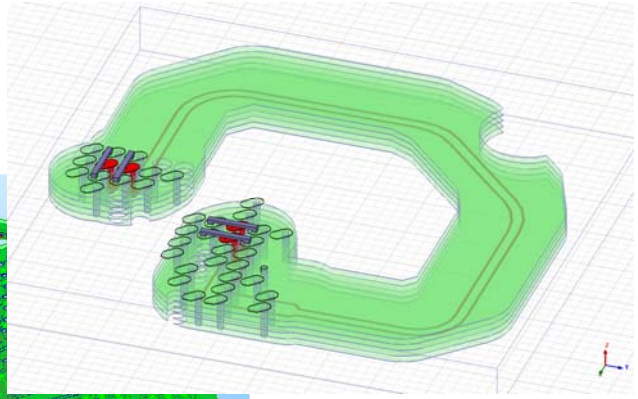
- Extract matrix parameters (S,Y, Z parameters), of signal nets and power distribution networks directly from EDA layout databases*.

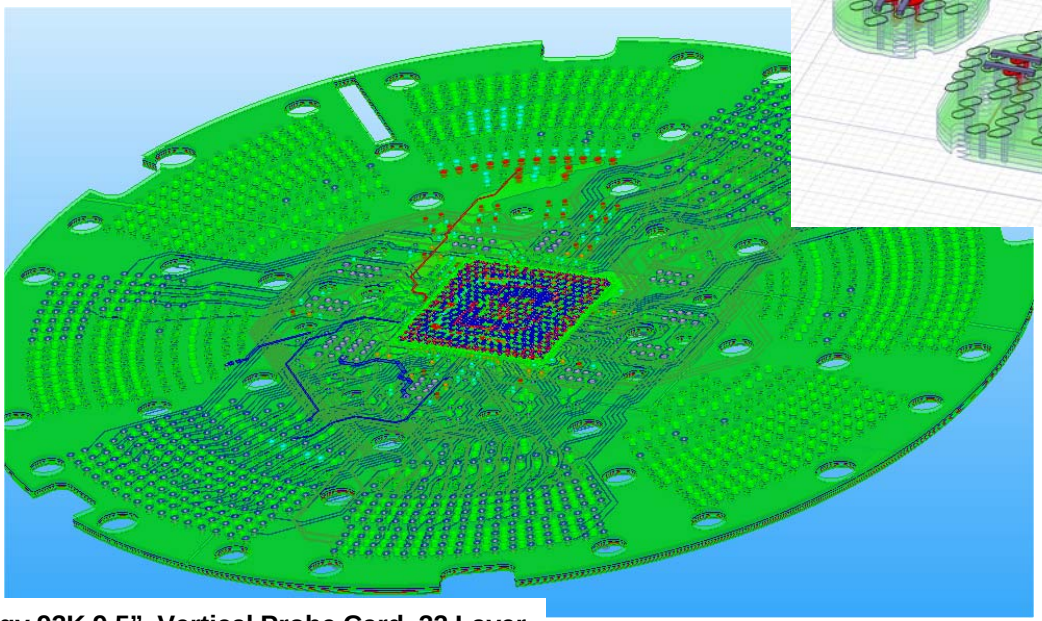
- Aids in the identification of signal-integrity and power-integrity problems and is critical to first-pass system success.

* ODB++ is used as a common transfer method. It must be verified if the ODB++ file created by a particular package is compatible.

Simulation
EDA Data Import

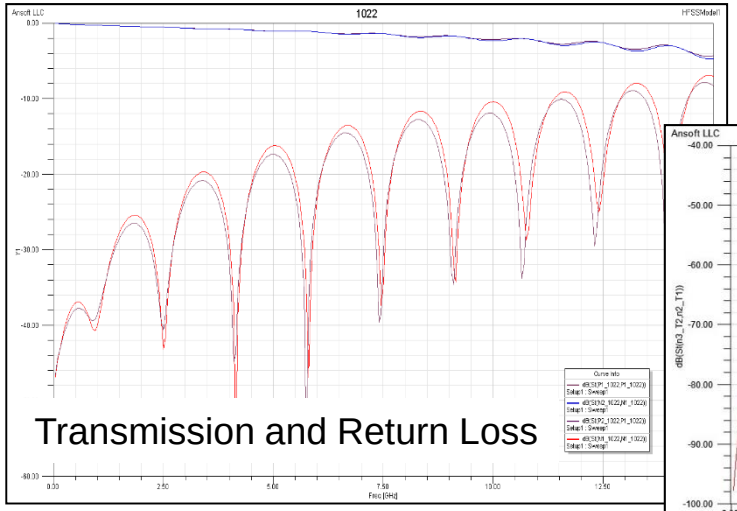
- ODB++ data files from the EDA Layout tool are directly imported.
  - Synergie-Cad can also provide simulation as a separate service.
- Measurement ports are place at the required points on the layout
- Extraction of matrix parameters (S,Y, Z parameters) for analysis.
- Cut-out sections of the layout to perform detailed 3D full-wave simulation of High-frequency and RF/microwave areas.



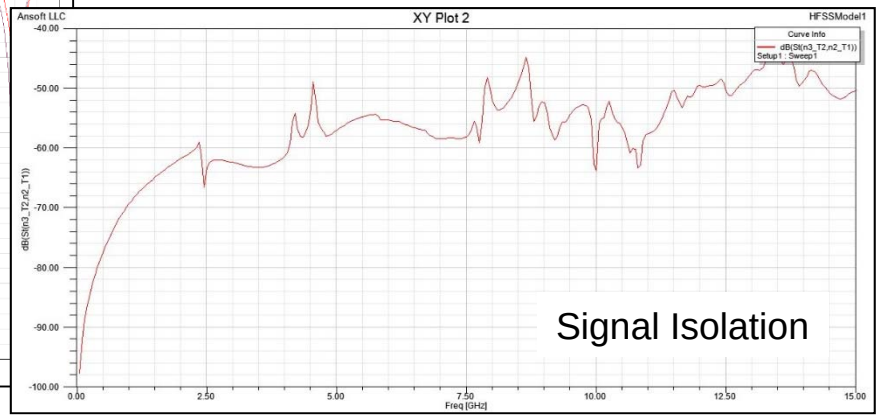


Verigy 93K 9.5”, Vertical Probe Card, 32 Layer

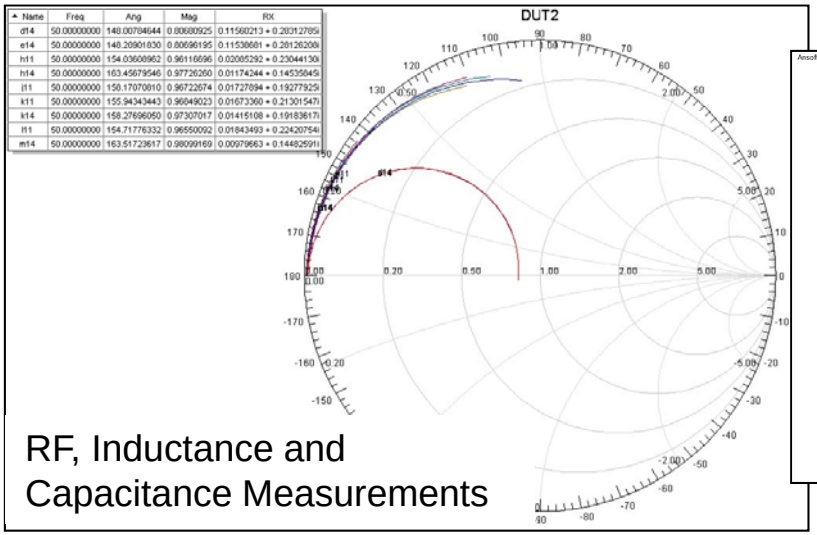
Simulation - Signal Integrity
Matrix Data (S,Y,Z, Parameters) Analysis



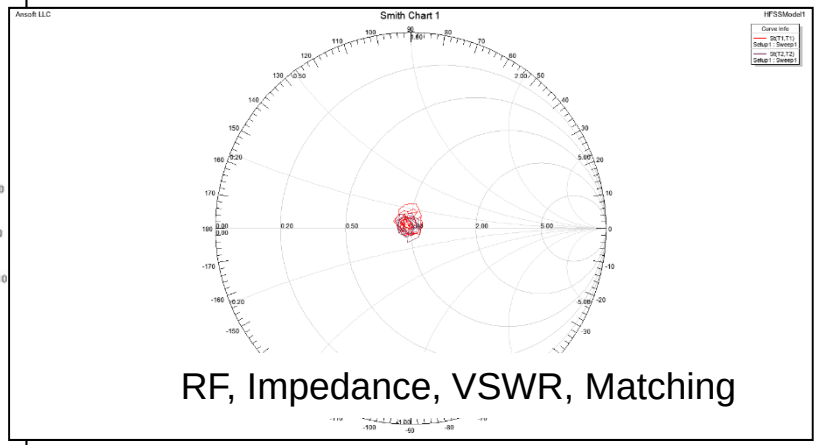
Transmission and Return Loss



Signal Isolation



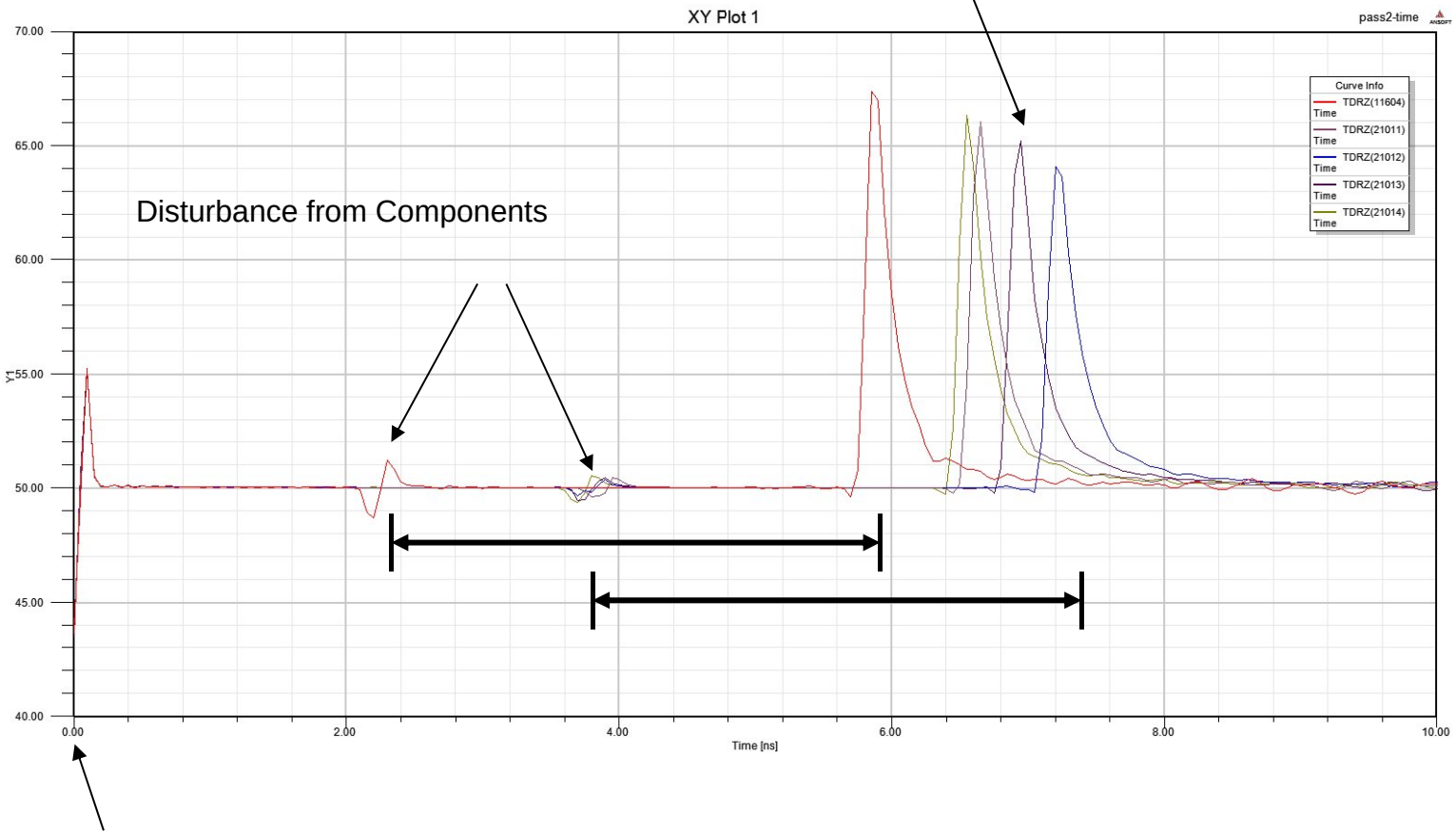
RF, Inductance and
Capacitance Measurements



RF, Impedance, VSWR, Matching

Simulation - Signal Integrity
TDR Analysis

Open circuit seen:
~7ns / 2 (return time of signal path) = ~3ns

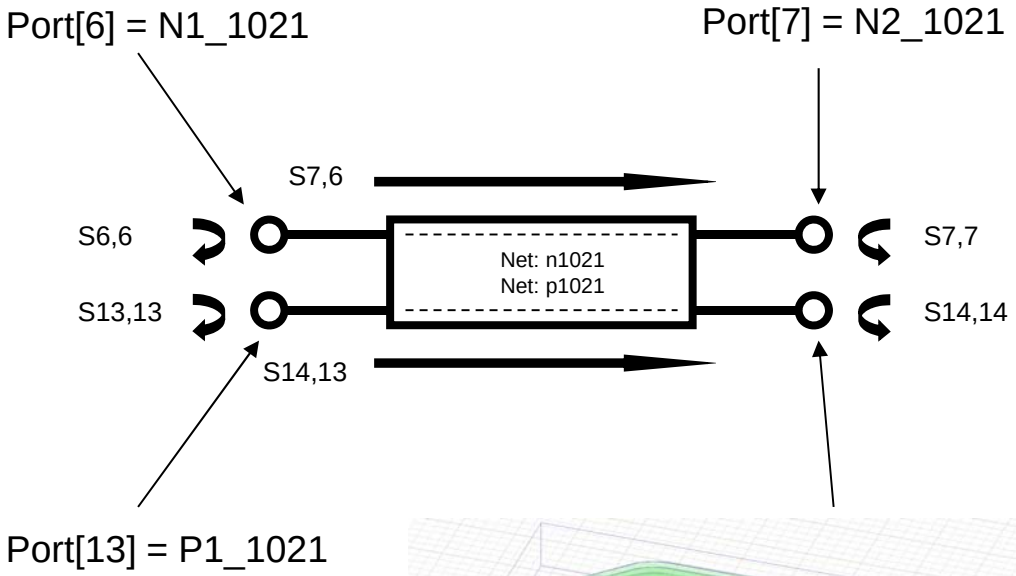


Tester pogo, t = 0ns

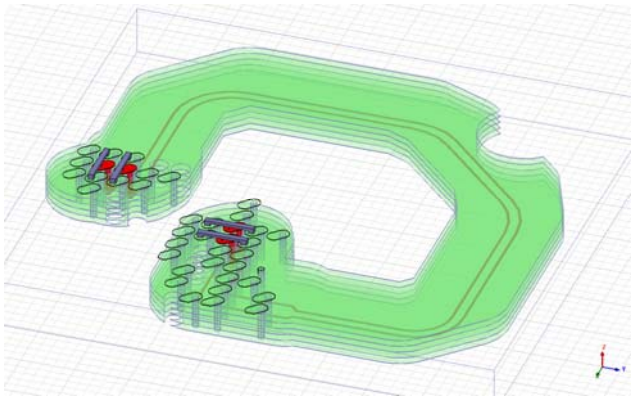
Simulation - Signal Integrity
Matrix Data Exported for use with Circuit Simulators

- Terminal data exported
- Port[1] = N1_1022
- Port[2] = P1_1022
- Port[3] = N2_1022
- Port[4] = N1_1025
- Port[5] = N2_1025
- Port[6] = N1_1021
- Port[7] = N2_1021
- Port[8] = N1_1024
- Port[9] = N2_1024
- Port[10] = P2_1022
- Port[11] = P1_1025
- Port[12] = P2_1025
- Port[13] = P1_1021
- Port[14] = P2_1021
- Port[15] = P1_1024
- Port[16] = P2_1024

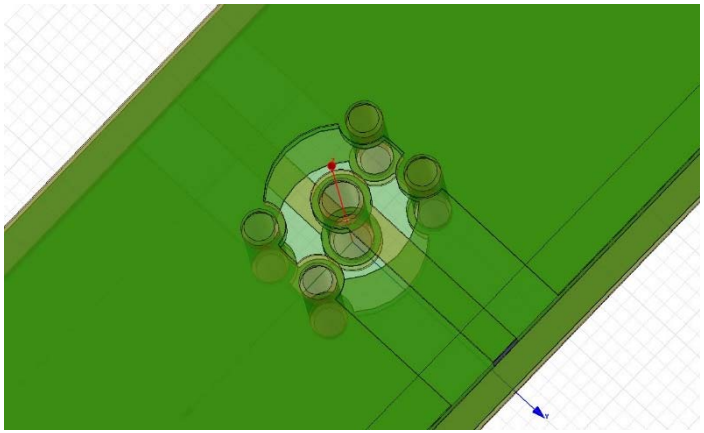
Example, Net 1021

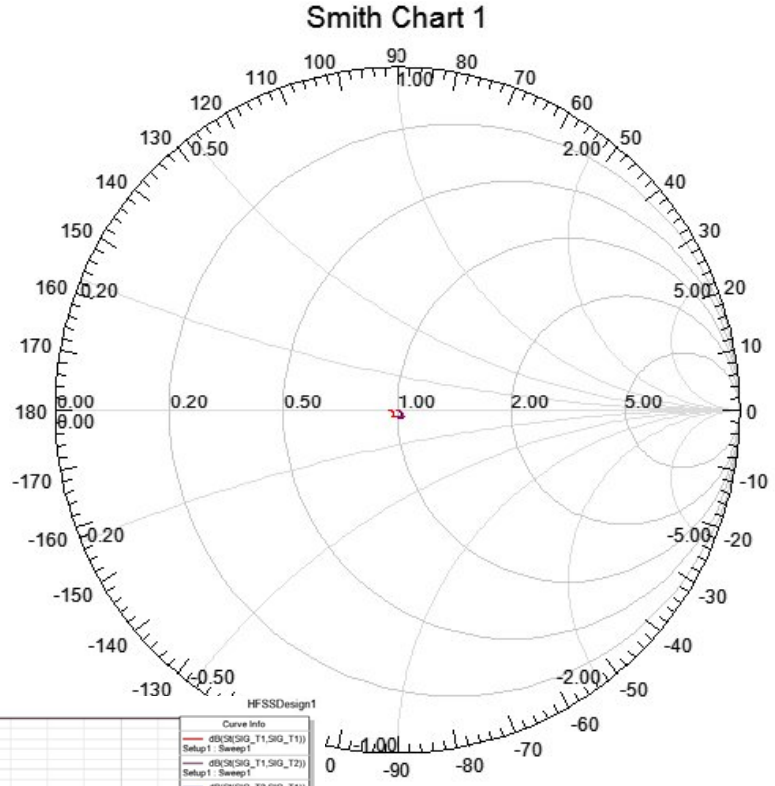


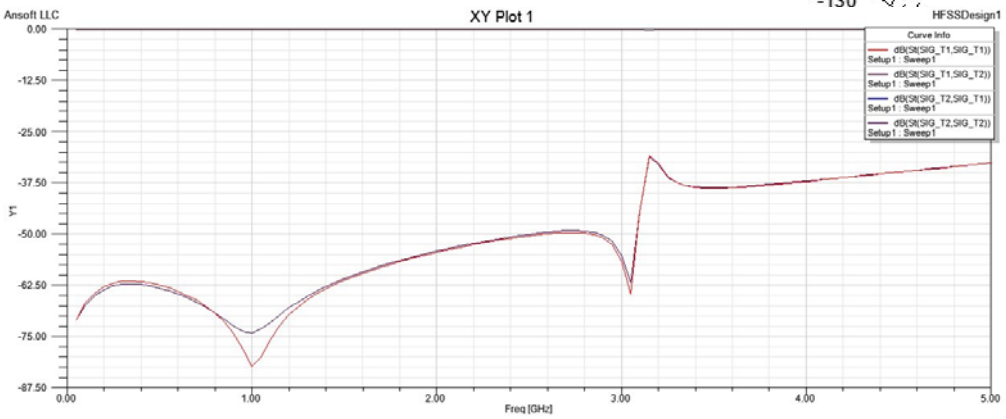
Touchstone S-Parameter data files



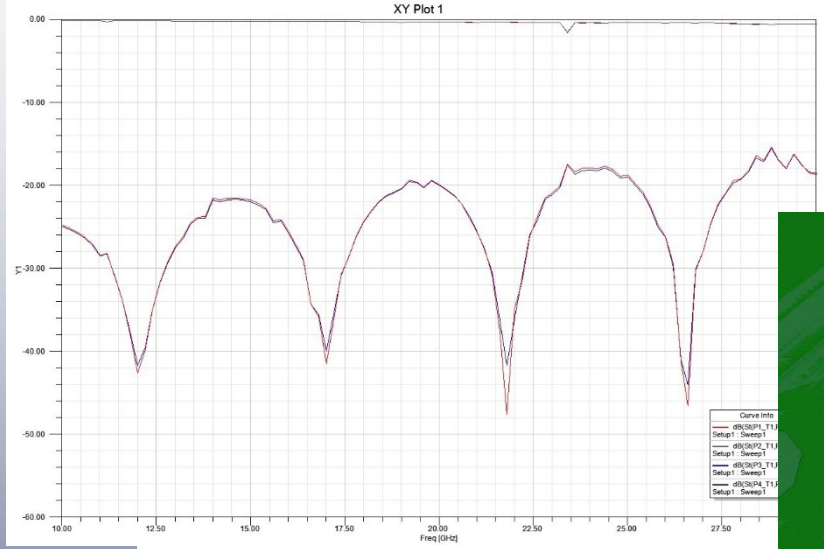
Example Simulation - Signal Integrity
Optimised 50 ohm Via, Transmission and Reflection Loss

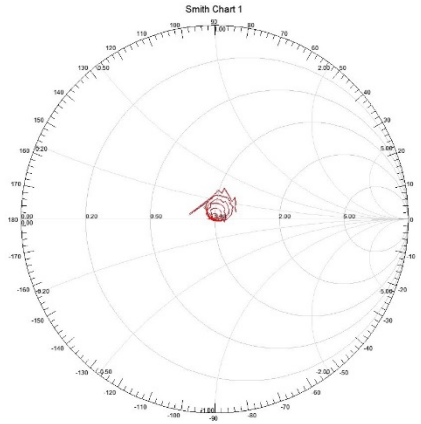




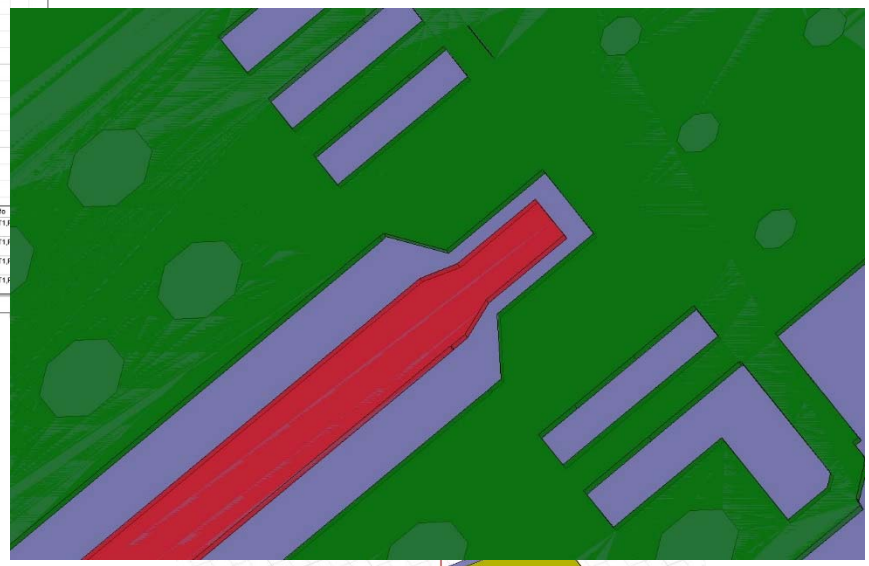


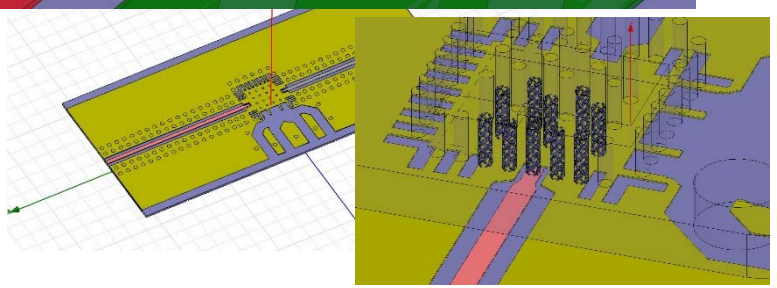
Example Simulation - Signal Integrity
Optimised Tapered RF Transformation



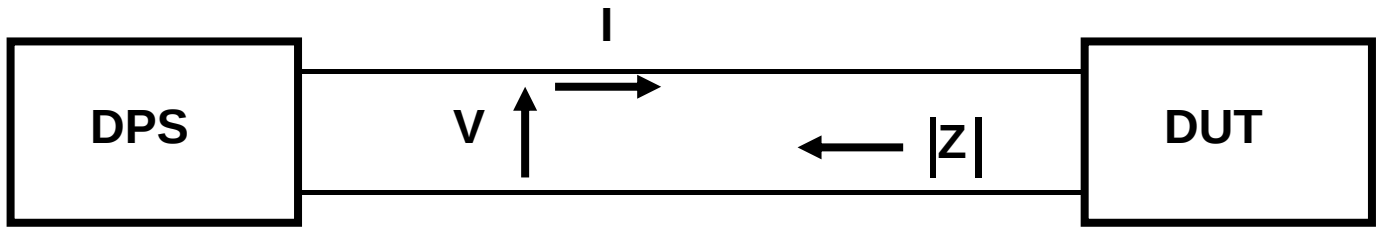


Optimised RF tapered transmission line impedance transformation, wideband, up to 30GHz.

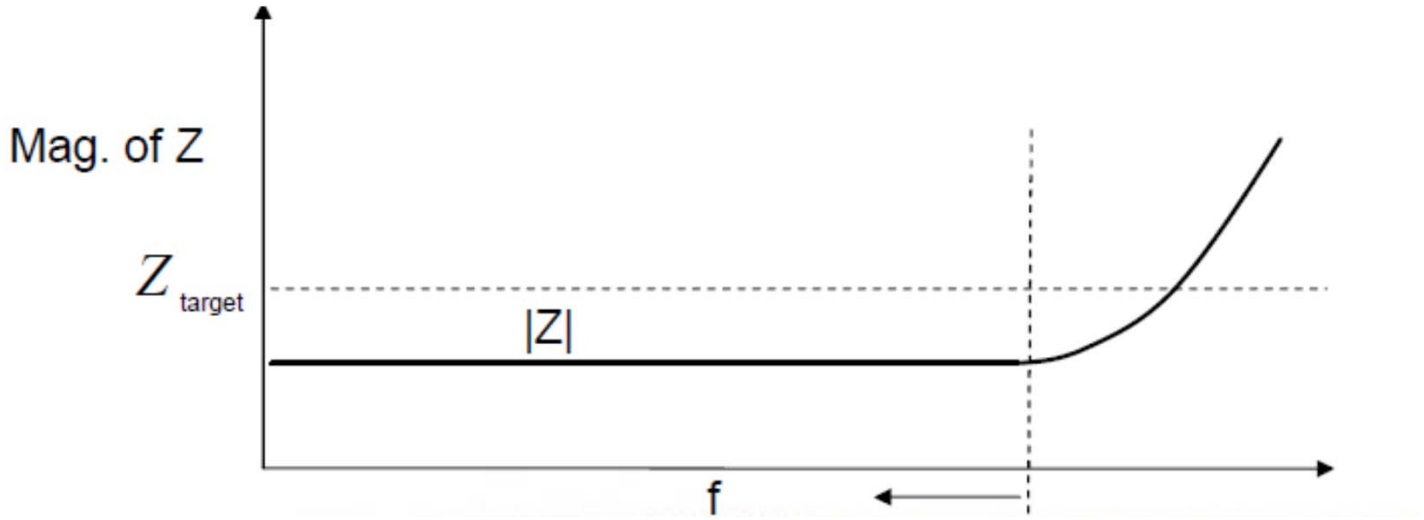




Simulation - Power Integrity
Basic Requirement: Target Impedance

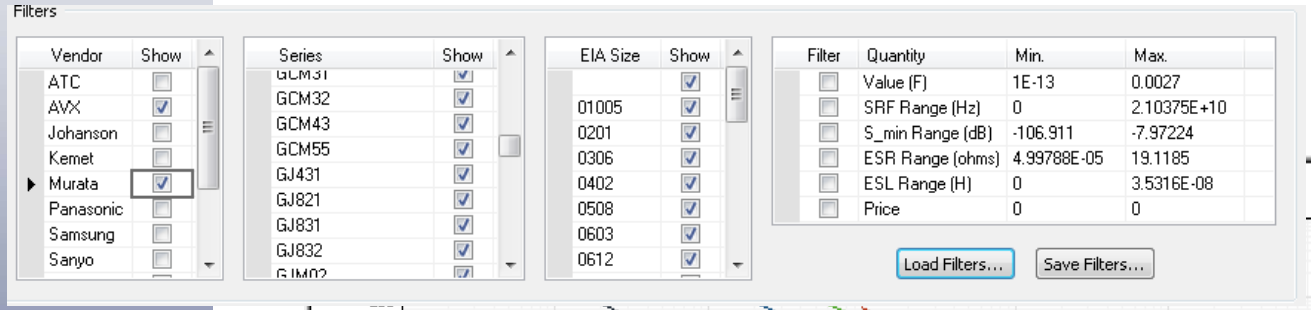


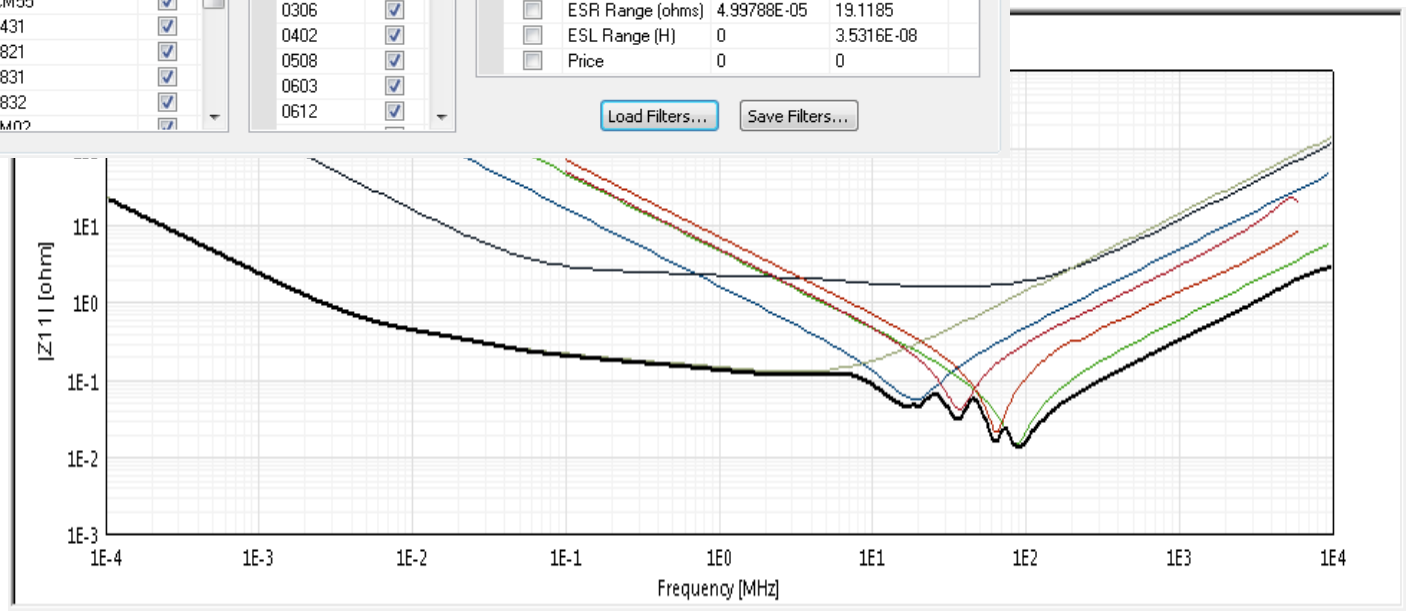
- The Impedance looking in the DPS from the device should be kept low over a broad frequency range.
- The Desired Frequency Range and Impedance Value is referred to as the Target Impedance.



Simulation - Power Integrity

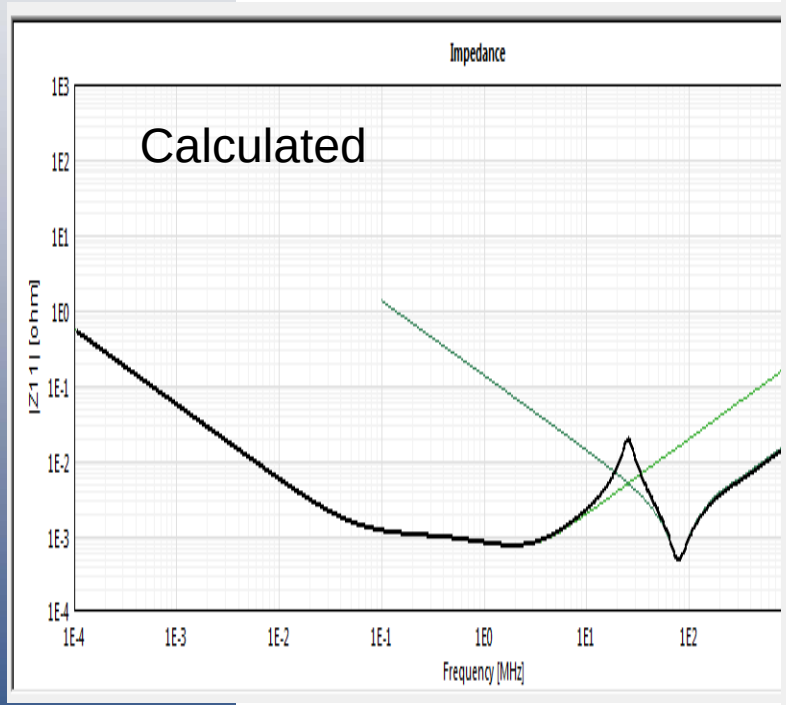
- Selecting the correct capacitance values is critical.
- Capacitors selection from a library of capacitor models.
- S-Parameter models can also be used.

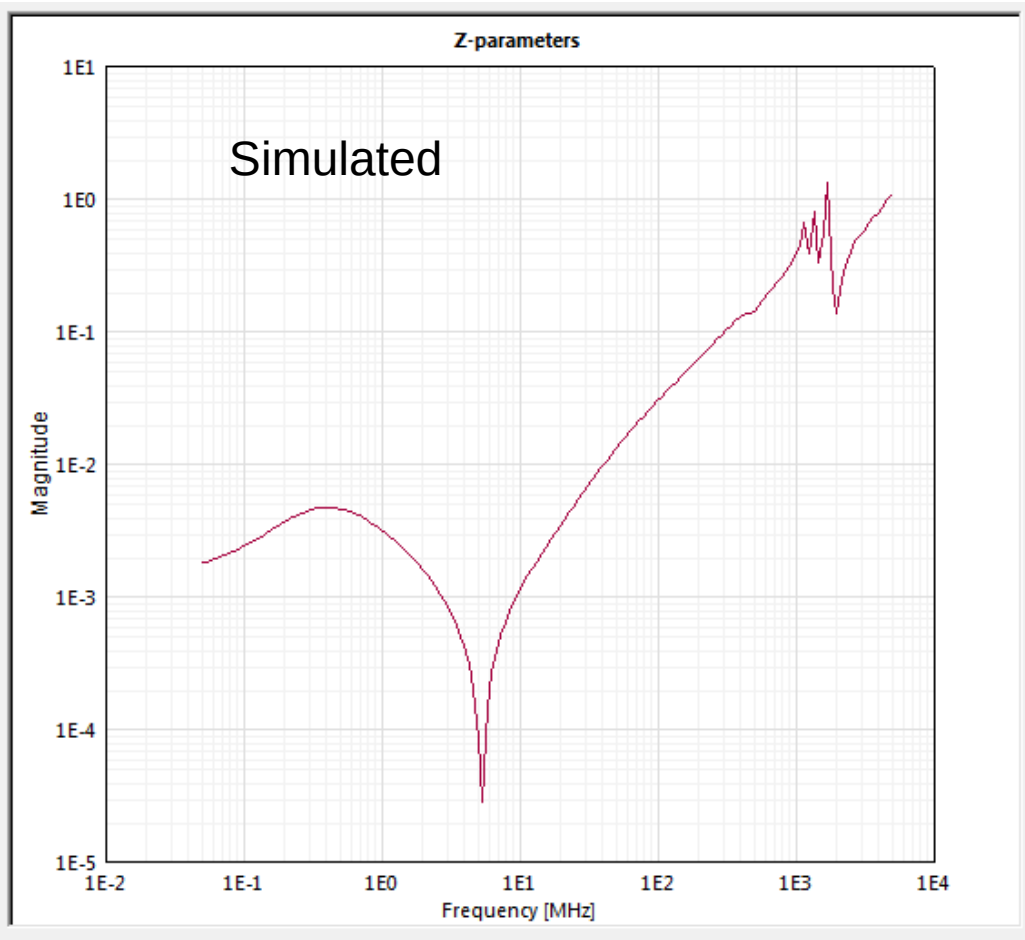




Simulation - Power Integrity

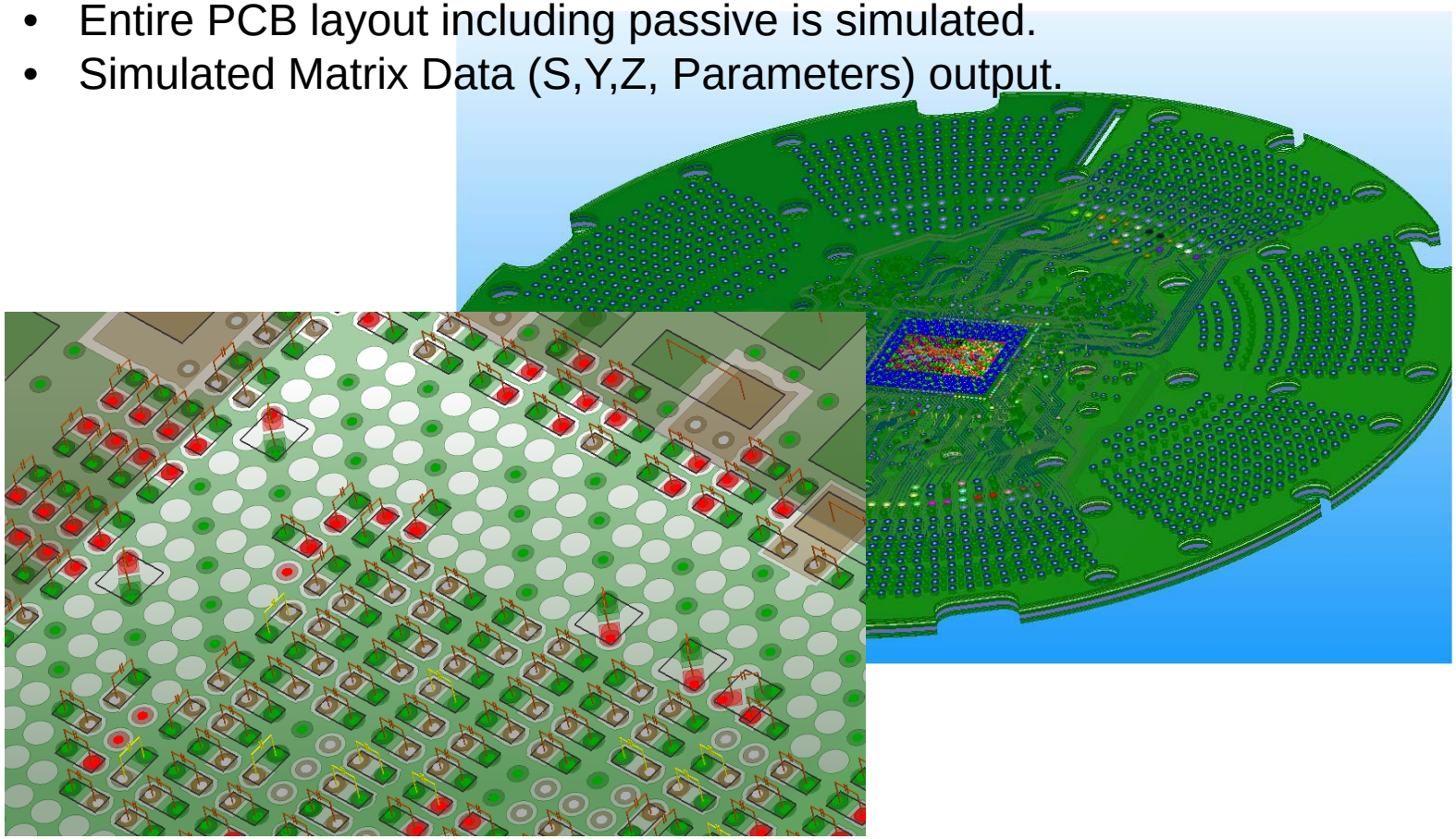
- However.. calculation of values alone is **not enough**.
- The effects of the layout **must be** taken into account.





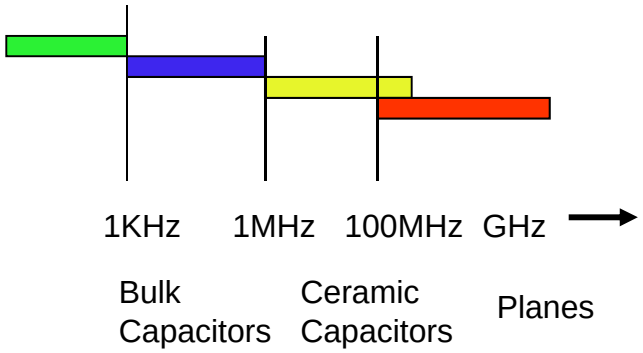
Simulation - Power Integrity
Analysis of Complete PCB Model

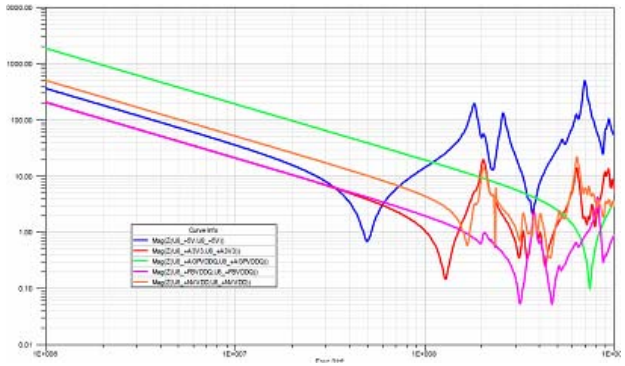
- Library of S-Parameter models for capacitor and inductors.
- Passives are fitted and at the SMD pads
- Entire PCB layout including passive is simulated.
- Simulated Matrix Data (S,Y,Z, Parameters) output.



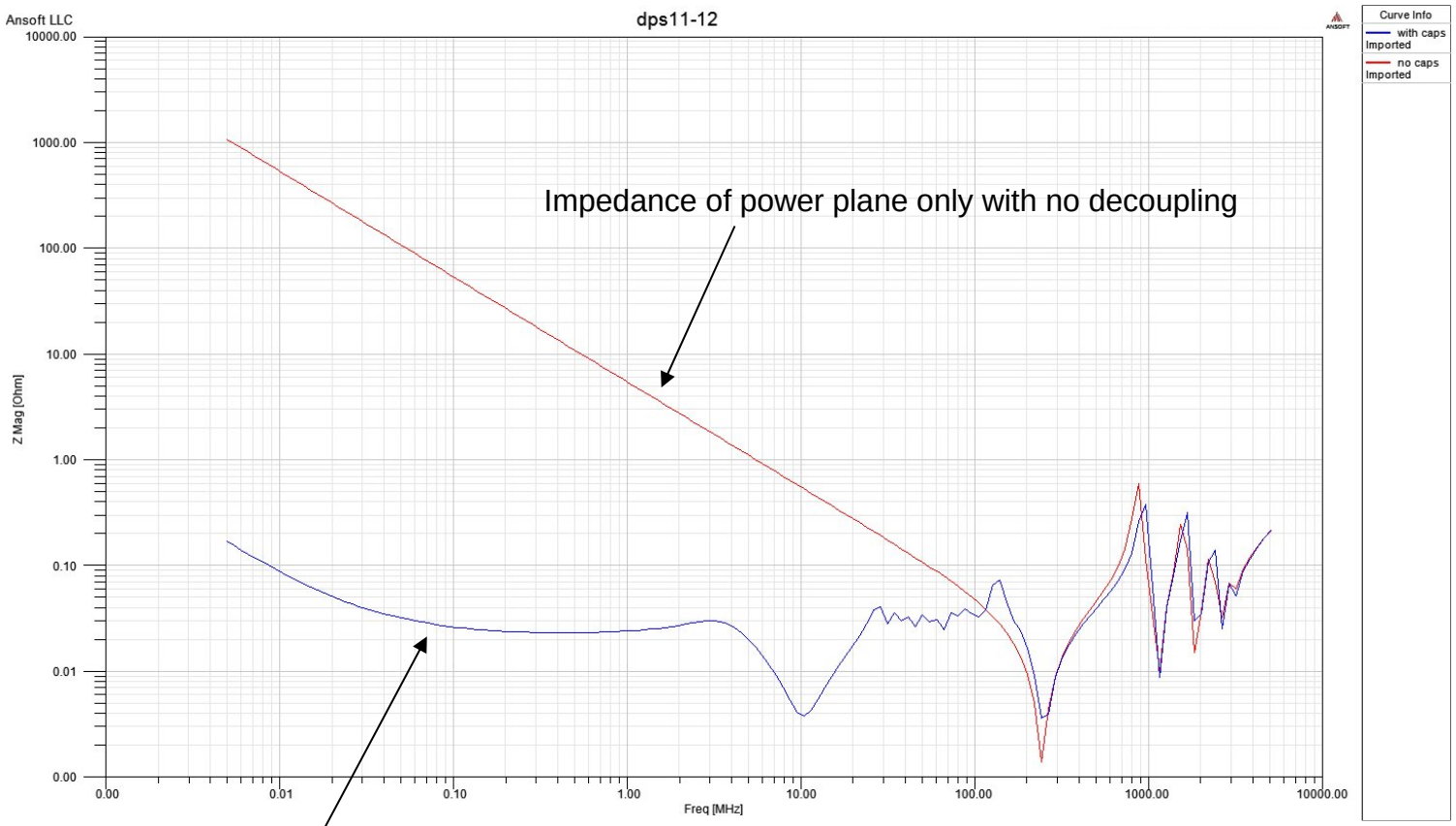
Simulation - Power Integrity
Placement effect on Target Impedance

- The effect of the placement and layout must be included in the overall model.
- Optimisation of the placement of components is required to minimise plane resonances.
- Optimisation of capacitor type / placement for the required performance over the desired frequency range.
- Optimisation of the layout to improve performance.
  - Inductance loops
  - Via length
  - Plane impedance





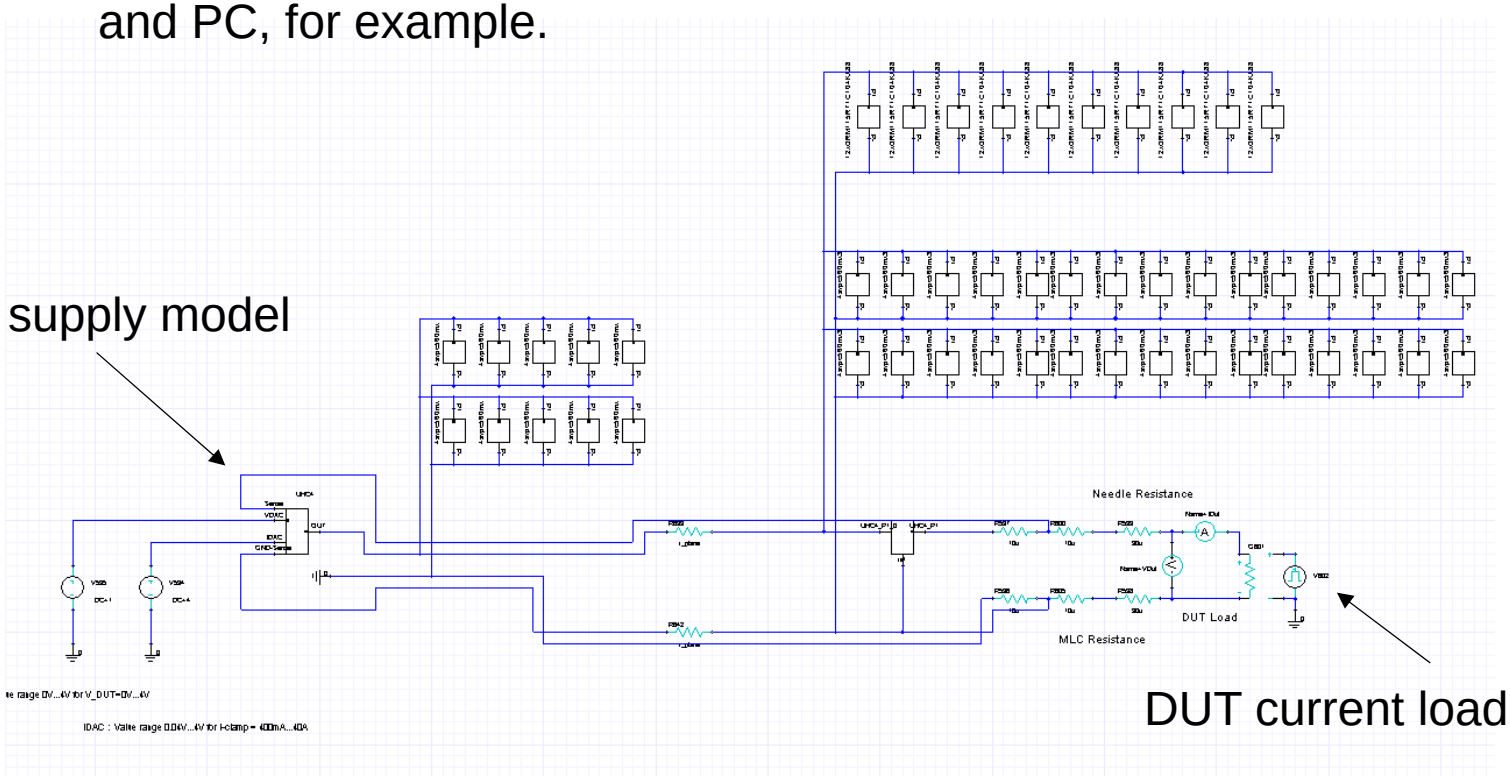
Example Simulation - Power Integrity
Resultant Matrix Data (S,Y,Z, Parameters)



Simulation - Power Integrity
Effect of Decoupling Network on Voltage Drop @ DUT

- Transient simulation to verify the effectives of the decoupling network.
- Circuit simulation of power supply using extracted board S-Parameters and decoupling.
- Cascade S-Parameter blocks to include any bulk decoupling of WPI and PC, for example.

Power supply model

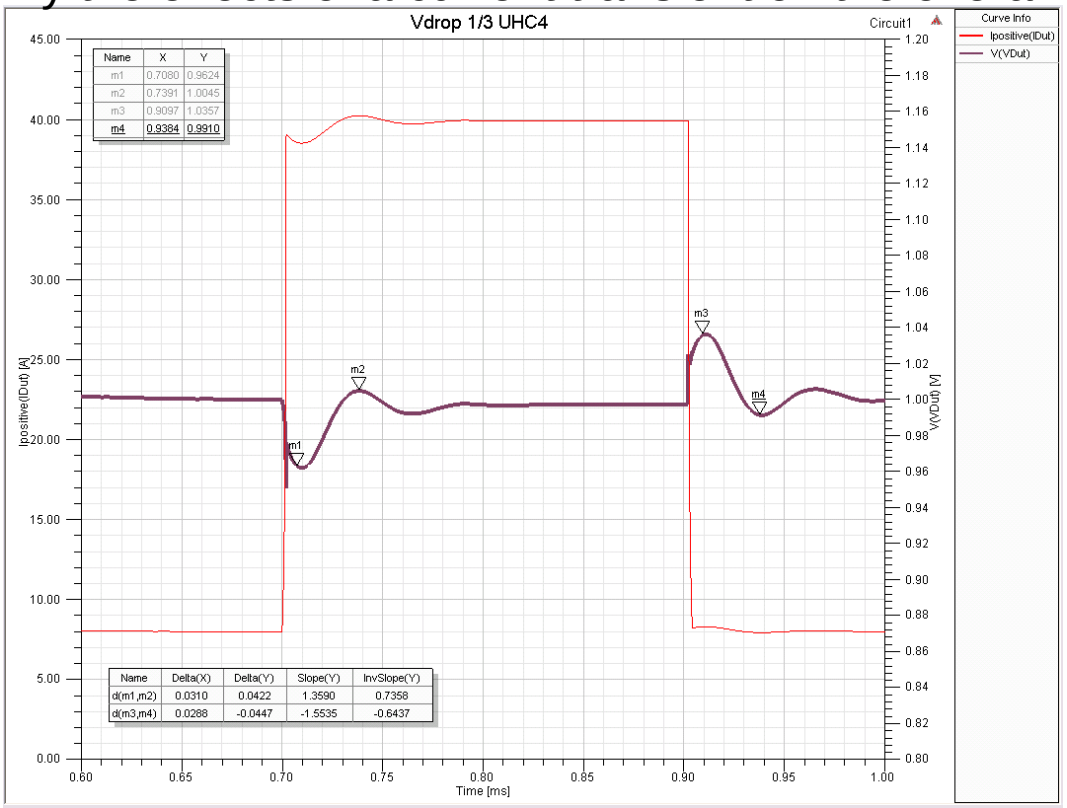


DUT current load

Simulation - Power Integrity

Effect of Decoupling Network on Voltage Drop @ DUT (cont.)

- Transient simulation to verify the effectives of the decoupling network.
- Power supply models of the tester hardware provided by the tester manufacturer.
- Simulate and verify the effects of a current transient on the overall network.



Thank You