Yeovil Electronic Developments

YED/PC/104/PANAVIA/T2/R2

PC/104 PANAVIA 2Tx/2Rx Interface

The PC104/PANAVIA/T2/R2 PANAVIA serial interface card is configured as a 16-bit Stack-through PC/104 interface and comprises of two independent transmitter channels that act as Bus Traffic Simulators and two independent receiver channels that provide Real Time Monitor and Data Acquisition functions. This card can be used in real time embedded applications or as a test simulator / Data Acquisition tool.

Transmitters

The transmitter executes autonomous instructions held in the dual port RAM. For each PANAVIA transmitter, either all the Tag values can be generated or just a sub-set. Tag data descriptors can be updated during transmission in real time without corruption of the transmitted data. All data is transmitted as standard 32-bit data with the Tag, Control bits and data fields in their correct positions as defined in the PANAVIA specification. Odd Parity is generated as standard.

Receivers

All received data is processed by the microprocessor and stored in the dual port RAM according to the channel number and Tag value. The data is stored in raw 26-bit format with the Tag, Control bits and data field preserved in their correct position as defined in the PANAVIA specification. The Parity is not checked, but is relayed in it's original state giving the option to check and handle errors, etc.

In addition, there is a channel Status register to provide information to the user about the state of the PANAVIA clock on each channel.

The received data is double buffered and read from alternate buffers. A PC Interrupt can be enabled/disabled on a channel by channel basis, and if enabled is asserted when TAG0 is received. A TAG0 counter for each channel provides a real time indication of the number of TAG0's received.

'C' Libraries

A 'C' Source code driver library accompanies this product and this is available as either a 16-bit or a 32-bit Microsoft Windows driver.

YED/PC/104/PANAVIA/T2/R2 Product Specification

- Two independent transmitter and receiver channels.
- Continuous bit synchronisation clock at 64Khz +/- 5% and 50% duty cycle (Tx)
- Dynamic update of transmitted data in real time
- 2 KB Dual port RAM for holding received Tag data words or Tag transmit tables
- Ping-Pong double buffering of received data.
- Transmission of sub-set of Tags, i.e. Transmission of Tag 21 thru Tag 25 only, etc.

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